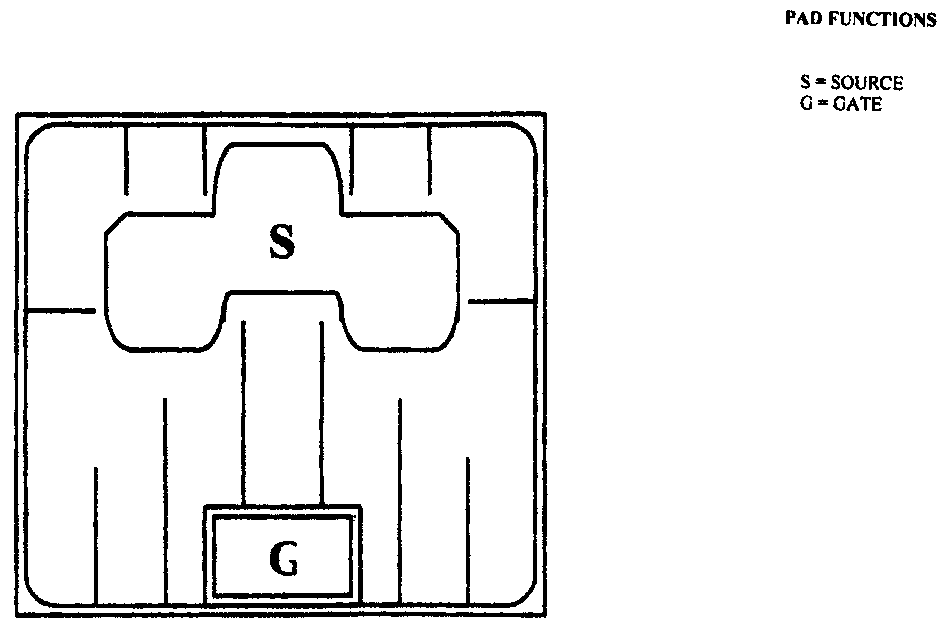
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.259”**

**.259”**

**Top Material: Al**

**Backside Material: TiNiAg**

**Bond Pad Size: G = .035” X .066”**

**Backside Potential: Drain**

**Mask Ref: IX5X**

**APPROVED BY: DK DIE SIZE .259” X .259” DATE: 8/17/16**

**MFG: IXYS THICKNESS .015” P/N: IXGD32N60B**

**DG 10.1.2**

#### Rev B, 7/19/02